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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,301	05/31/2000	Frank P. Helms	1001-0119	3171

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ZAGORIN O'BRIEN GRAHAM LLP
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/584,301	HELMS, FRANK P.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-14,16-21,24,26,27 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 24* is/are allowed.

6)☒ Claim(s) *1-7,9,14,19-20,26,27 and 31-33* is/are rejected.

7)☒ Claim(s) *10-13 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 14, 16-18, 20, 21, 24, 26, and 31 have been amended, and claims 15, 22, 23, and 25 have been canceled by Applicant. Claims 1-7, 9-14, 16-21, 24, 26, 27, and 31-33 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 26-27 and 31-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 26 and 31 recite that the first region or memory control circuit is initialized by the reset signal, but the reset signal 708 is not connected to and does not affect the CPU 703 or memory controller 704, only the logic at 707. It is also unclear how a reset signal, which may apparently have two states, may hold a memory control signal at a value and also initialize a circuit, it would appear that opposite states of the signal would be required to do these two things. Claims 27 and 32-33 incorporate this limitation by dependency.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 26-27 and 31-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 26 and 31 recite that the reset signal initializes the first region of memory control circuit. It is unclear what is meant by the term "initialize" since the reset signal is not connected to controller 704 and no further explanation is given of what occurs to initialize (other than the memory controller begins driving the CKE line low, which is what it does when powered). Claims 27 and 32-33 incorporate this limitation by dependency.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-7, 9, 14, 19-20, 26, and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Baweja et al., US 6,212,599 B1.

8. As to claims 1-7, 19-20, Baweja discloses *a method for and computer system controlling a self refresh state of memory, comprising supplying a memory control signal* (CKE 330, Fig. 3) *to the memory from a first integrated circuit* (210, Fig. 2) *according to an operational state* (first operation mode, via SDCKE 240 and 320, Fig. 3), *supplying the memory control signal from another location* (310, Fig. 3) *when in a power savings*

state to maintain the self refresh state (via SCKE and 320, Fig. 3). See Abstract, Figs. 2-3, col. 2 line 40 to col. 3 line 5, col. 4 lines 23-28, and col. 4 line 64 to col. 5 line 22. In each case the clock enable signal is supplied from its source (the clock enable signals SDCKE or SCKE), and merely passed by AND gate 320 (which will pass any active low signal from input to output).

9. As to claims 9 and 14, Baweja discloses the claimed invention substantially as described above with regard to claim 1. The limitation that the first integrated circuit is isolated from the memory during the power savings state, by disabling a switch coupling them is met by the AND gate 320 coupling to the CKE 330 signal. That is, when first state machine 310 outputs low SCKE (the recited switch enable signal that turns off the switch) in response to going into sleep mode, CKE 330 remains low regardless of state of the first integrated circuit output SDCKE 240, effectively isolating SDCKE and disabling it's connection to CKE.

10. As to claims 26 and 31-32, Baweja discloses the claimed invention substantially as described above with regard to claims 1 and 14. The limitation that the signal that holds the control signal is an asserted reset signal is met by the SCKE signal of Baweja, with SCKE low considered asserted. The limitation that the reset signal initializes as recited is ignored (as applied to the 35 USC 112 rejections above), but the low signal also is considered to initialize the gate 320, since this allows the source of SDCKE to be powered down, then powered back up, without affecting the output CKE.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al., US 6,212,599 B1, in view of Henkhaus et al., US 6,654,895 B1.

13. As to claim 27, Baweja does not disclose a S3 suspend to RAM state. However, this state was previously known in the art. See Henkhaus col. 1 lines 57-65, which describe the S3 state as cutting all power except that to save system memory, and that this state is ideal to achieve an instantly available computer since it saves the most power while allowing fast restart. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use this state, because it was a known state to achieve maximum power savings while still allowing fast restart.

14. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al., US 6,212,599 B1.

15. As to claim 33, Baweja does not disclose the integrated circuit includes the memory control circuit and the CPU. However, it has long been known in the art that the combination of elements into fewer elements, such as integration of a plurality of elements into a single chip, has benefits of lowering cost and a possible improvement in speed due to smaller circuit scale. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the memory controller and CPU on

the same circuit, because of the long known benefits from integration of lower cost, space requirements, and possible improved performance.

Response to Arguments

16. Applicant's arguments filed June 15, 2005 have been fully considered but they are not fully persuasive.

17. Regarding claims 1 and 14, Applicants have argued that in Baweja the signal CKE 260 is always supplied from the controller 220, and that signals SDCKE 240 and SCKE are not supplied to the memory. However, this circuit is essentially the same as the one shown by Applicant in Figs. 7 and 8A. Here Applicant attempts to apply a double standard by stating that the clock enable signal is supplied from the AND gate 320 of Baweja, and formed from two other signals (while in the present application the clock enable is described as an input to as well as an output from the AND gate). Examiner agrees with the standard of Applicants own invention here; since the AND gate does not generate the signal, and since the signal is active low and active low signals are merely passed by the AND gate, it is maintained that the clock enable output of the AND gate of Baweja (the recited memory control signal) is properly interpreted as being supplied from the clock enable inputs to the AND gate, and thus from those clock enable signal sources.

18. Regarding claim 9, Applicants argue that the SCKE signal of Baweja cannot be both the switch enable signal and the memory control signal (if SCKE is the switch enable signal, that it cannot also be said to supply the memory control signal). Examiner notes that the claim does not state the "other location" supplies the memory

control signal, only "controlling" it from that location, and that a switch enable signal may certainly be interpreted as controlling the memory control signal.

19. Regarding claims 26 and 31, Applicants argue that the SCKE signal of Baweja is not a reset signal and does not initialize the first region. However, the reset signal of the present invention is not connected to and does not affect the memory control circuit 704 (see 35 USC 112 rejection above). Assuming the Applicant intends initializing the region to mean initializing the logic at 707, Examiner disagrees, and maintains that the signal SCKE of Baweja does everything that the claimed reset signal does. It holds the memory control signal at the first value during power savings, and it initializes the AND gate equivalently to the claimed invention since it holds the signal while allowing the first control signal input to be powered up and supply the control signal. It is also noted that simply calling the signal a "reset" signal has no importance, since Applicant has stated that any signal could be used; therefore any signal that does what the recited "reset" signal does may be interpreted as the recited reset signal.

20. Applicants arguments regarding the previous 35 USC 103 rejections are convincing.

Allowable Subject Matter

21. Claims 21 and 24 are allowed.

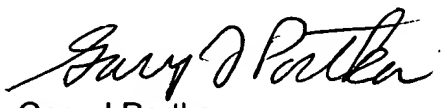
22. Claims 10-13 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Gary J Portka
Primary Examiner
Art Unit 2188

GARY PORTKA
PRIMARY EXAMINER

July 25, 2005